

**REMARKS**

- Claims 1-21 were pending in the application
- Claims 1-21 stand as rejected
- Claims 1-12 stand as objected to
- Claims 1, 7, 13, and 17 are independent claims
- Claims 1, 7, 13, and 17 have been amended

**A. REJECTION UNDER 35 U.S.C. §112, FIRST PARAGRAPH**

Claims 1-12 stand rejected under 35 U.S.C. 112, first paragraph. On page 2 of the Office Action, the Examiner asserts that the specification lacks enablement with respect to claimed limitation "selecting a bit" recited in claims 1-3, 6-9, 12. Specifically, the Examiner argues that "[t]he specification lacks enablement with respect to claimed limitation 'selecting a bit' recited in claims 1-3, 6-9, 12. The specification fails to clearly describe the claimed invention with respect to selecting a bit from a memory, so a person skilled in the art would be able to carry out the invention." For reasons explained below, Applicants respectfully traverse these rejections.

Applicants submit that one of ordinary skill in the art at the time of the invention would clearly have sufficient knowledge to carry out the invention based on Applicants' specification. That is, Applicants submit that the feature of "selecting a bit" was commonly known in the art well before the time of the invention. For example, in the summer of 1946 at the Moore School of Electrical Engineering at the University of Pennsylvania, Jan Rajchman of RCA Laboratories gave a lecture on the Selectron tube for early computers which specifically covered an example of "Selecting a Bit" (See "Vol. IV, Lecture 43, 23rd August 1946" in The Moore School

Lectures: Theory and Techniques for Design of Electronic Digital Computers. (1985) Martin Campbell-Kelly and Michael R. Williams, editors: Cambridge, Massachusetts: The MIT Press and Tomash Publishers. ISBN 0-262-03109-4.) Accordingly, Applicants assert that claims 1-3, 6-9, and 12 are allowable under 35 U.S.C. §112, first paragraph.

**B. REJECTIONS UNDER 35 USC §112, SECOND PARAGRAPH**

Similarly, the Examiner asserts that claims 1-12 are indefinite under 35 U.S.C. §112, second paragraph, as failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Specifically, the Examiner asserts that claims 1-3, 6-9, 12 recite the limitation of "selecting a bit" and that there is insufficient antecedent basis for this limitation in the claims, because it is not clear whether the selected bit is the same bit or different bits. (Office Action, page 4). For reasons explained below, Applicants respectfully traverse these rejections.

Applicants assert that it is clear that the selected bit is from the selected memory array. Claim 1 specifically recites the features of "... storing the selected bit from the selected memory array." That is, the bit that is stored is the selected bit **from the selected memory array**. Claims 2-3, 6-9, and 12 recite similar features. Accordingly, Applicants believe that claims 1-3, 6-9, and 12 particularly point out and distinctly claim the subject matter of selecting a bit. For at least these reasons, Applicants assert that claims 1-3, 6-9, and 12 are allowable under 35 U.S.C. §112, second paragraph and respectfully request withdrawal of same.

**C. REJECTION OF CLAIMS UNDER 35 USC § 101**

Claims 1-12 stand rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. Specifically, claims 1 and 7 were rejected as reciting an abstract idea without any tangible results.

On page 4 of the Office Action, the Examiner alleges that the steps, as recited in claims 1 and 7, of selecting and storing a bit constitute an abstract idea without any tangible results, and without further reciting practical applications, such as a structure or apparatus for implementing the steps. For reasons explained below, Applicants disagree with the Examiner's assertion.

Applicants respectfully submit that storing a bit is a tangible result. Specifically, Applicants submit that storing a bit is a tangible result in that the bit may be read at some time later. Moreover, Applicants submit that the description of the present invention makes it clear that the stored bit is part of the data that may be employed to compare data written, which Applicants submit is a useful and tangible result. Specifically, the specification notes that "[t]he data output from a memory array may be compared to the data written to the memory array to identify a failure or defect in the memory array. (Page 5). In spite of this clearly tangible result, Applicants have amended the independent claims for the sole purpose of expediting prosecution.

Without acceding to the Examiner's arguments, Applicants have amended the independent claims to include the features of "wherein an outcome of the ABIST test is determined based on the stored selected bit" or the like. Applicants assert that such features are, over and above the already tangible results from storing a bit, clearly tangible

in that a test result is based on the stored bit. Accordingly, Applicants assert that independent claims 1 and 7 as amended are allowable under 35 U.S.C. §101.

**D. REJECTION OF CLAIM UNDER 35 USC §102**

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,853,597 (hereinafter "Jain"). The Examiner asserts that Jain discloses a method and apparatus for an integrated circuit, IC 100, having a BIST control unit 102 for testing a plurality of memory banks (104a-d). For reasons explained below, Applicants traverse these rejections.

Independent claims 1, 7, 13, and 17 recite features such as "receive a bit during an ABIST test from each of the plurality of memory arrays; and storing the selected bit from the selected memory array" or the like. The Examiner argues that such features are taught by the "(faulty word, BitFa-d) from each of the plurality of memory banks (104a-d) in the BIST control unit 102, Fig. 1." (Office Action, page 7). For reasons explained below, Applicants disagree.

In contrast to such features, Jain teaches using a **plurality** of comparator units. In the Summary of the Invention, Jain states that

[t]he invention relates generally to ICs with a plurality of memory banks. More particularly, the invention relates to built-in self-testing of memory banks. In one embodiment, a BIST control unit is provided for testing the plurality of memory banks simultaneously. The BIST control unit **is coupled to a plurality of comparator units**. In one embodiment, a comparator unit is coupled to a memory

bank for comparing a test pattern written to the memory bank against data read from the memory bank.

(Emphasis is added). In more detail, Jain teaches that

...**a** comparator unit 106 is coupled to **a** memory bank 104 to facilitate parallel testing. The comparator unit compares the test patterns written to memory against the actual data read from memory. A failure occurs when a mismatch is found. The test patterns TData are provided **to the comparator units simultaneously** by the BIST control unit, and comparison is carried out in parallel to reduce the amount of time required for testing. A variety of test patterns, such as the march, checkerboard, wordline stripe or blanket patterns, may be provided. The test patterns may be hard-coded in the BIST control unit or programmed during the test mode.

(Jain, column 2, lines 9-20). Applicants also submit that there is nothing else in Jain to suggest the features of "...selecting one of the plurality of memory arrays; and storing the selected bit from the selected memory array" or the like. Accordingly, Applicants assert that all the features of independent claims 1, 7, 13, and 17 are not taught or suggested by Jain.

In addition to the above distinctions, Applicants note that the present Application may desirably reduce real estate by reducing the number of latches, in apparent contrast to Jain. As noted in the background of the present Application, "[b]ecause each observation latch occupies a large amount of space on an IC chip, including an observation latch for each memory array of the IC chip may consume a

sizeable amount of real estate or floor plan area of the IC chip. Accordingly, methods and apparatus for testing integrated circuits that consume less chip real estate would be desirable." (Background). The specification further teaches that "...the novel IC chip 200 may require fewer latches to perform an ABIST test than the conventional IC chip 100. By reducing the number of latches included in the IC chip on which an ABIST test 20 may be performed, less chip real estate is consumed." (Page 6, lines 16-20). In contrast to the teachings of the present invention, Jain teaches employing a 'plurality of comparator units' which Applicants submit may use a sizeable amount of real estate.

Accordingly, Applicants assert that independent claims 1, 7, 13, and 17 are allowable under 35 U.S.C. §102(e) over Jain.

#### **E. CONCLUSION**

Since the Applicants assert that all the independent claims as amended are in condition for allowance and all remaining claims properly depend from the independent claims, Applicants assert that all claims are allowable.

Applicants do not believe a Request for Extension of Time is required but if it is, please accept this paragraph as a Request for Extension of Time and authorization to charge the requisite extension fee to Deposit Account No. 04-1696. Applicants do not believe any additional fees are due regarding this Amendment. However, if any additional fees are

required, please charge Deposit Account No. 04-1696.

Respectfully Submitted,



Steven M. Santisi  
Registration No. 40,157  
Dugan & Dugan, PC  
Attorneys for Applicants  
(914) 332-9081

Dated: September 20, 2007  
Tarrytown, New York